QP CODE : 58022

LINEAR INTEGRATED CIRCUITS SOLUTION

(CBCGS SEM – 4 MAY 2019)

BRANCH – ELECTRONICS AND TELECOMMUNICATION

Q.1 Attempt any 4 questions:

a) Give Ideal Characteristics of op-amp and give their practical values. (05)

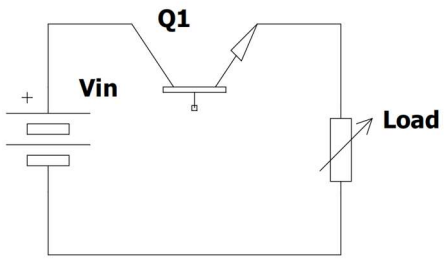
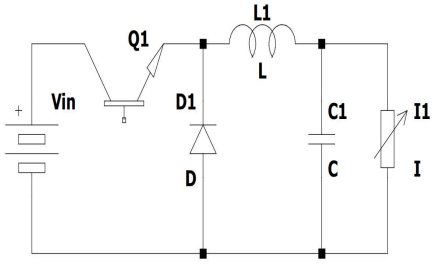
SOLUTION:

Various characteristics of an Ideal and practical op-amp are as follows

Sr.No.	Characteristics	Practical op-amp value	Ideal op-amp value
1	Input Resistance (R_i)	2 MΩ	Infinite
2	Output Resistance (R_o)	75 Ω	0
3	Voltage gain (A_V)	2×10^5	Infinite
4	Bandwidth B.W.	1 MHz	Infinite
5	CMRR	90 dB	Infinite
6	Slew rate (S)	0.5 V/µs	Infinite
7	Input offset voltage (V_{ios})	2 mV	0
8	PSRR	150 µV/V	0
9	Input bias current (I_B)	50 nA	0
10	Input offset current (I_{ios})	6 nA	0

b) Compare linear and switching voltage regulator. (05)

SOLUTION:

Sr.No.	Parameter	Linear Regulator	Switching Regulator
1	Circuit Diagram		
2	Region of operation	Active region	Saturated or Cut-off

3	Switching	No switching	Transistor acts as a switch
4	Complexity	Less	High
5	Efficiency	Low (40%)	High (90%)
6	Switching frequency	Very low	Very high (25kHz)
7	Switching losses	Zero	Very high
8	RFI/EMI	Absent	Very high
9	Component stress	High	Very high
10	Regulation	Excellent	Good
11	Cost	Lowest	Moderate
12	Size/Weight	Large/Bulky	Small/Light weight
13	Power handling capacity	Low	High

c) Design a circuit for $V_o = V_1 + V_2$ using single op-amp and few resistors. (05)

SOLUTION:

The above circuit can be designed by using non-inverting summing amplifier.

If V_1 and V_2 are the input voltages the output of non-inverting summing amplifier is given as

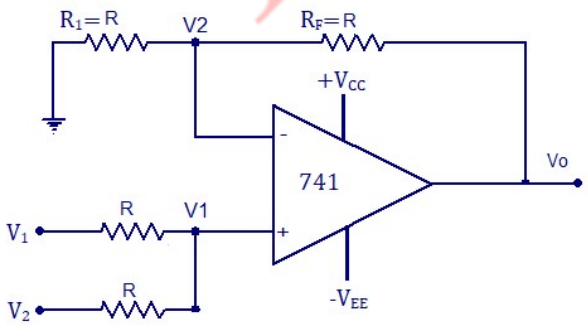
$$V_O = A_{VF} \times \frac{V_1+V_2}{2}$$

So, to get desired output A_{VF} should be equal to 2.

But, $A_{VF}=1+\frac{R_F}{R_1}$

Hence, for $R_F=R_1=R$, $A_{VF}=2$

Hence the circuit can be designed as follow



d) What are the advantages of switch capacitor filters? (05)

SOLUTION:

1. The primary advantage of switched capacitor filters is that they can be easily implemented on an integrated circuit.

2. Performance similar to an analog RC op-amp based filter can be obtained using a switched capacitor topology, while avoiding the need for an ADC, DSP, and DAC on a chip.

3. Switched capacitor circuits use capacitors and switches to emulate the behavior of resistors. Additionally, the frequency response is determined by the ratio of the capacitors, so even low frequency filters can be easily realized on-chip.

4. The real benefit of switched capacitor filters is for IC implementations such that while the absolute value of capacitances and resistances have a poor tolerance, the matching between similar devices is very good. This makes it possible to implement relatively high precision analog filters on a chip.

In an integrated circuit, you would choose a switched capacitor filter for the following reasons:

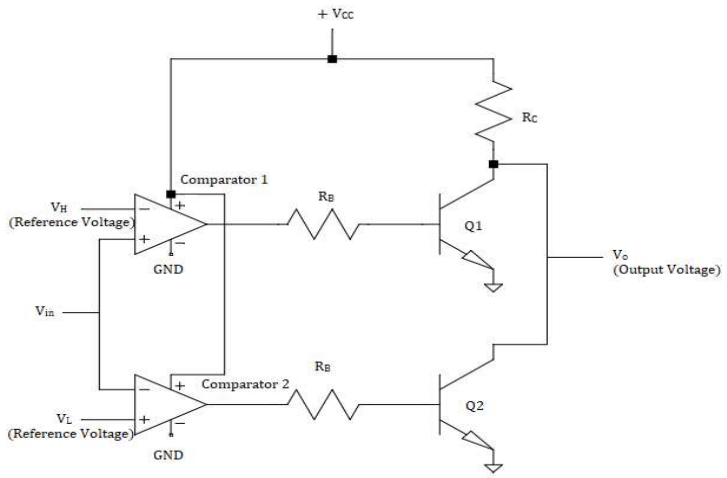
- Minimizing chip area is a priority
- You will not be doing significant digital processing on the chip
- The output of the DSP would be an analog signal

e) Explain op-amp as Window detector. (05)

SOLUTION:

1. Op-amp can be used as a window detector so as to detect whether the input voltage V_{in} lies within a specified range (between V_H and V_L). This range is referred as *Window.*

2. A window detector circuit can be obtained as follows using 2 op-amps and 2 transistors that operates as switch.



3. The outputs of 2 comparators are connected to the transistors and output voltage is collected from common collector terminal of the transistors.

4. If V_{in} is between the two reference voltages i.e. $V_L < V_{in} < V_H$ then the outputs of both the comparators will be low. So both the transistor will be in off state and hence output will be high else low.

5. Hence, the three output conditions are as follows

i. $V_o = +V_{CC}$ for $V_L < V_{in} < V_H$
ii. $V_o = V_{CE\,(sat)}$ for $V_{in} < V_L$
iii. $V_o = V_{CE\,(sat)}$ for $V_{in} > V_H$

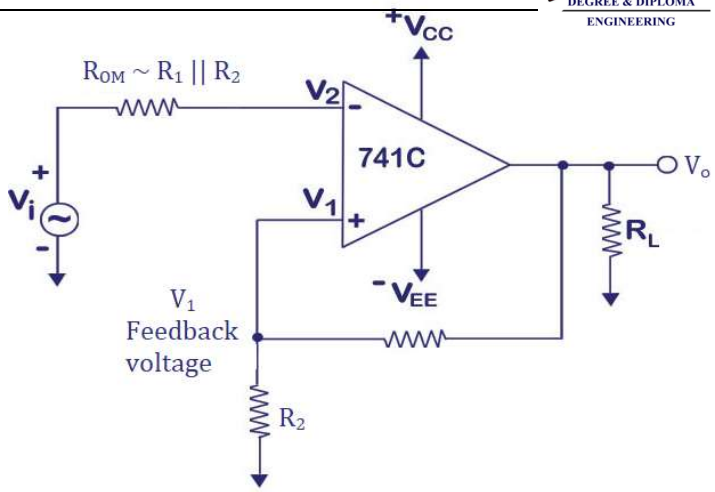
Hence, when the output is high (i.e. applied V_{CC} is obtained at output) if the input voltage is in the range else low.

Q.2.

a) With the help of a neat diagram and voltage transfer characteristics explain the working of an inverting Schmitt trigger. Derive the expression for its threshold levels. (10)

SOLUTION:

1. The inverting Schmitt trigger is as shown below



2. The resistance divider formed by R_1 and R_2, connected between the output and non-inverting terminal of the op-amp introduces the positive feedback.

3. The Schmitt trigger is basically an inverting comparator with positive or regenerative feedback introduced. Hence also known as regenerative comparator.

4. External input V_{in} is applied to the inverting input of the op-amp. The resistor R_{OM} is called offset minimizing resistor and is equal to parallel combination of R_1 and R_2.

5. The reference voltage is V_1 developed across R_2. This reference voltage is not fixed but its sign and amplitude depends upon output voltage because,

$$V_1=\frac{R_2}{R_1+R_2}\times V_o$$

6. The 2 different triggering/threshold voltages are defined for the Schmitt trigger as follows:

- Upper threshold voltage V_{UT}
- Lower threshold voltage V_{LT}

7. The output voltage will change its state every time input voltage cross threshold levels.

8. The upper threshold level is defined as value of V_{in} which forces a transition from $+V_{sat}$ to $-V_{sat}$ in output voltage.

Similarly the lower threshold value is defined as value of V_{in} which forces output voltage to change from $-V_{sat}$ to $+V_{sat}$ in output voltage.

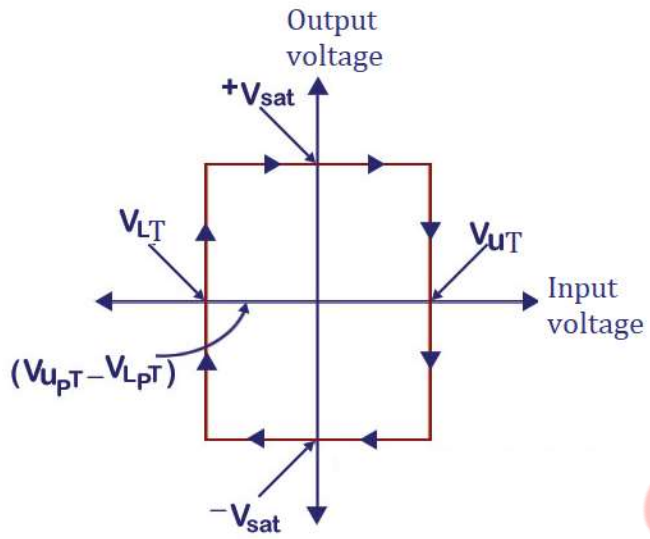
9. Thus upper and lower threshold/trigger voltages can be given as

$V_{UT} = \frac{R_2}{R_1+R_2} \times V_{sat}$

$V_{LT} = \frac{R_2}{R_1+R_2} \times -V_{sat}$

Thus the magnitude of upper and lower threshold voltage is same but has opposite sign hence also known as symmetrical Schmitt trigger.

10. Transfer characteristics of inverting Schmitt trigger is a shown



Such that when, $V_{in} < V_{UT}$ then $V_o = +V_{sat}$

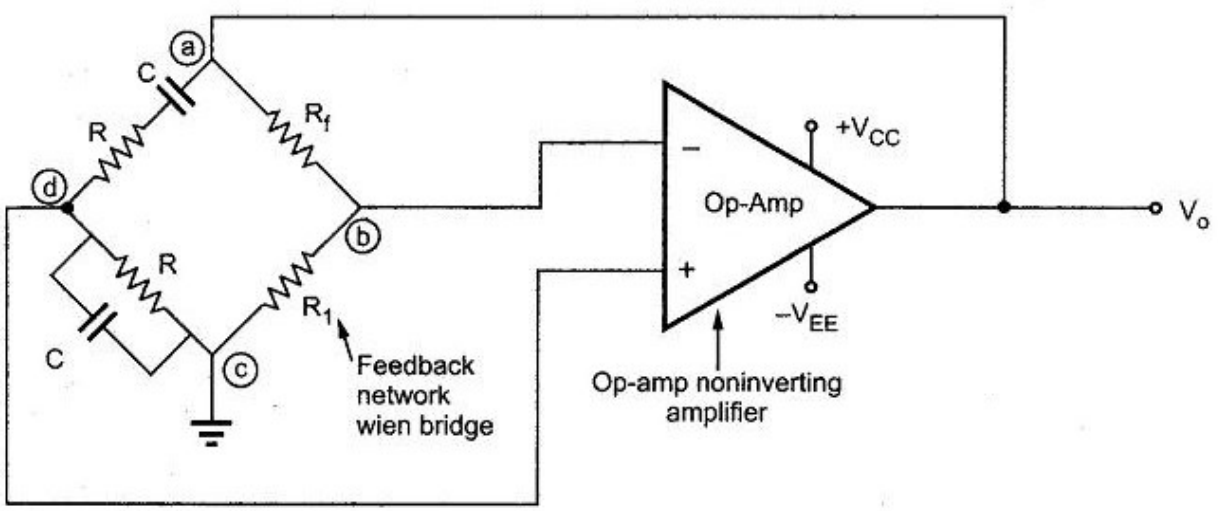
$V_{in} > V_{LT}$ then $V_o = -V_{sat}$.

b) Draw a neat circuit diagram of Wien bridge oscillator using op-amp. Derive its frequency of oscillation. What are the values of R and C for frequency of oscillation to be 965 Hz? (10)

SOLUTION:

Working of Wien bridge oscillator

1. A Wien bridge oscillator with a non-inverting op-amp amplifier is as shown below



2. The Wein bridge has 4 arms. The arm AD which contains a series of combination of R and C, whereas arm CD contains a parallel combination of R and C.

This value of R and C is used to decide the value of oscillator frequency such that

$$f = \frac{1}{2\pi R}$$

3. The resistors R_F and R_1 are used to generate a reference voltage which remains constant independent of the frequency f.

4. The AC input voltage is applied between the points A and C of the bridge. When Wien bridge is used in oscillator circuit, the feedback voltage is applied between these points.

5. The AC output of the bridge is obtained between the points B and D which is connected as inputs of the non-inverting amplifier.

6. The value of feedback factor β depends upon the frequency. At oscillator frequency f_o the phase shift introduced is zero and thus value of feedback factor β is 1/3.

7. According to Barkhausen criteria the phase shift around the loop should be zero and loop gain should be greater than 1.

i.e. $|A\beta| \geq 1$

substituting $\beta=1/3$, we get $A \geq 3$.

Therefore the gain of the amplifier should be greater than or equal to 3.

8. Data: f_o= 965 Hz

Let C=0.01 µF

Since $f_o = \frac{1}{2\pi R}$

$R= \frac{1}{2\pi f_o C} = \frac{1}{2\times\pi\times965\times0.01\times10^{-6}}$ = 16.49 kΩ

C=0.01 µF, R=16.49 kΩ

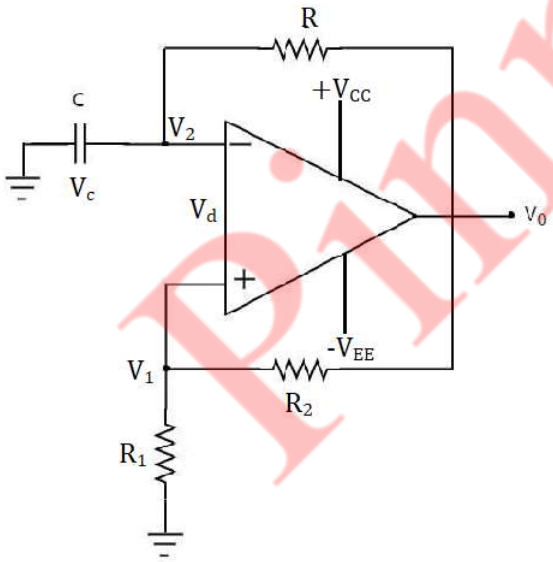
Q. 3.

a) Draw the circuit diagram of a square and triangular waveform generator using op-amp and explain its working with the help of waveforms. (10)

SOLUTION:

A. Square wave generator:

A square wave generator using op-amp can be designed as follow



1. Let the voltage on the capacitor C is zero when power is applied to the circuit. Therefore initially the voltage at the inverting terminal is zero i.e. $V_2=V_C=0$.

2. Due to some output offset voltage present at output of op-amp, the voltage V_1 at non-inverting terminal is non zero and will have a value that depends on the

output offset voltage and values of resistance R_1 and R_2. Hence differential voltage V_d is equal to V_1.

Operation:

The operation of square wave generator can be divided in 2 parts:

1. Operation from 0 to t_1:

- The voltage V_1 will start driving the op-amp output towards saturation. For example if V_1 is positive initially then it will drive the comparator output to $+V_{sat}$ if V_d is positive.
- With op-amp output equal to $+V_{sat}$ the capacitor C starts charging through R and V_C starts increasing exponentially in the positive direction.
- The voltage V_1 across R_1 is given by

  $V_1 = \frac{R_1}{R_1+R_2} \times V_{sat}$

Hence $V_1 = \beta.V_{sat}$ where, $\beta = \frac{R_1}{R_1+R_2}$

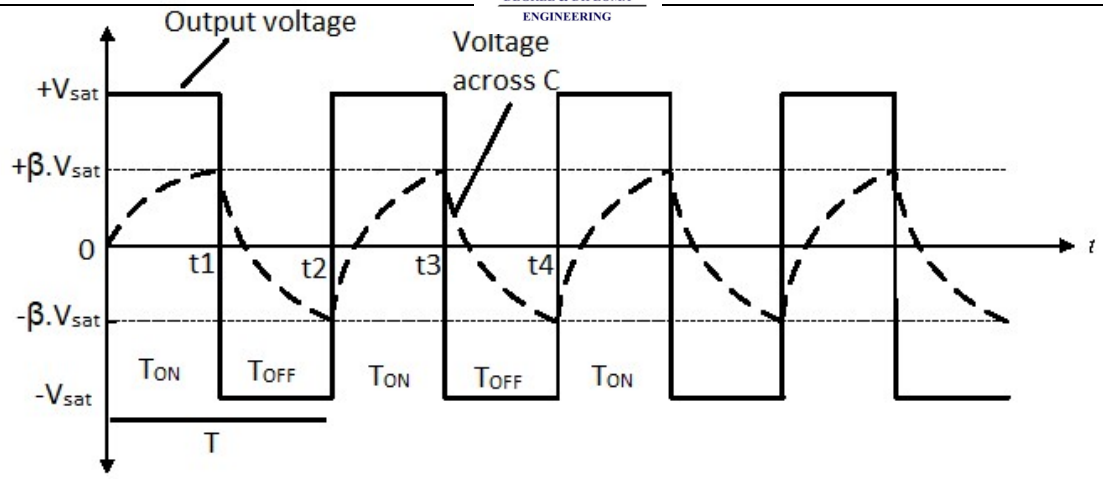
2. Operation from t_1 to t_2

- At $t=t_1$ the capacitor voltage V_C is equal to $\beta.V_{sat}$. As soon as the voltage on C i.e. V_2 becomes slightly more than V_1, the differential voltage V_d changes its polarity and op-amp output will suddenly switch to a negative saturation i.e. $-V_{sat}$.
- Due to this sudden changeover voltage V_1 also becomes negative as

  $V_1 = \frac{R_1}{R_1+R_2} \times -V_{sat}$

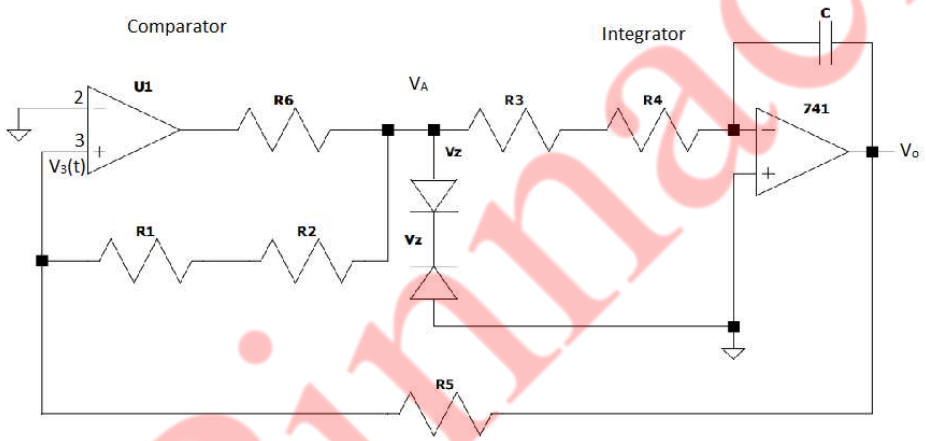
  Hence, $V_1 = -\beta.V_{sat}$
- The capacitor C starts discharging through R and the output stage of the op-amp.
- As soon as V_C becomes slightly more negative than V_1, the differential voltage polarity will be at $t=t_2$ reversed and the op-amp output will suddenly switch to a positive saturation i.e. $+V_{sat}$.

This process will repeat itself to generate a square waveform at the output of op-amp.



B. Triangular wave generator:

A triangular wave generator using op-amp can be obtained by a combination of comparator and integrator as shown



- At $t=t_0$ let the output of comparator be equal to $+V_{sat}$. Hence the voltage at point A will be clamped to $+V_Z$.
  $V_A = +V_Z$
- Let us assume the integrator output at $t=t_o$ is positive equal to
  $V_o(t_o) = \frac{R_5}{R_1+R_2} \times V_z$
  That means the capacitor is charged to this voltage with its right plate positive.
- Due to positive voltage $+V_Z$ at point A the capacitor starts charging linearly through the resistors R_3 and R_4. This will charge the left plate of the capacitor towards appositive voltage. Therefore the net voltage

on the capacitor starts decreasing linearly.

- The charging current in the interval time t_o to t_1 is given by

  $I^+ = \frac{V_Z}{R_3+R_4}$

- The voltage at non-inverting terminal of the comparator is given by superposition theorem

  $V_3(t) = \frac{R_5\ Vz}{(R_1+R_2+R_5)} + \frac{(R_1+R_2).V_o(t)}{(R_1+R_2+R_5)}$

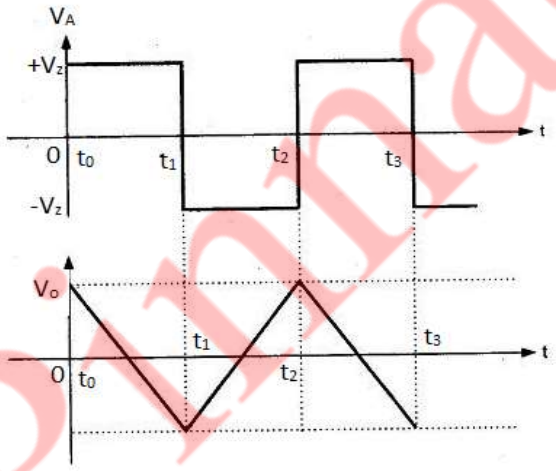
- At instant $t=t_1$ the instantaneous voltage at non-inverting terminal of comparator i.e. $V_3(t)$ is given by above equation.

  Due to this the voltage at point A will be clamped to $-V_Z$ and the capacitor will discharge through R_3 and R_4.

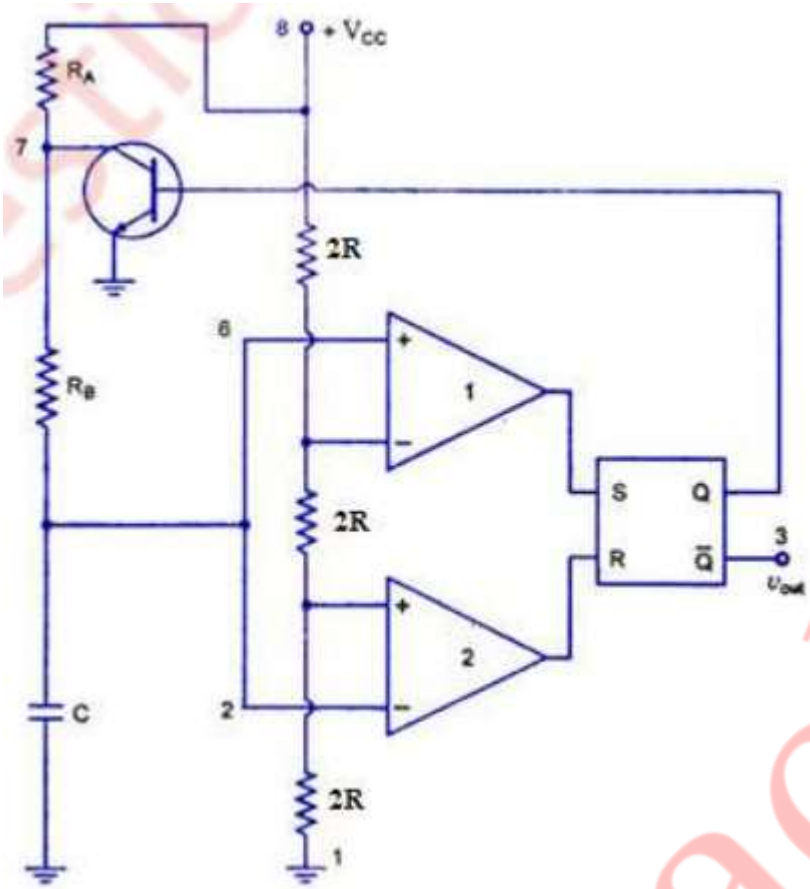
- The capacitor voltage now starts becoming positive. The discharging current is given by

  $I^- = \frac{-V_Z}{R_3+R_4}$

  As this current is constant, the voltage on the capacitor i.e. output voltage increases linearly.



b) The circuit given in following figure is similar to that of internal diagram of IC555 with slight modifications in the internal resistance to value 2R. Analyze this circuit and draw the waveforms at output terminal V_{out} and across the capacitor C. Comment on the duty cycle of output waveform when i) R_A is less than R_B ii) R_A is equal to R_B, and iii) R_A is greater than R_B. (10)



SOLUTION:

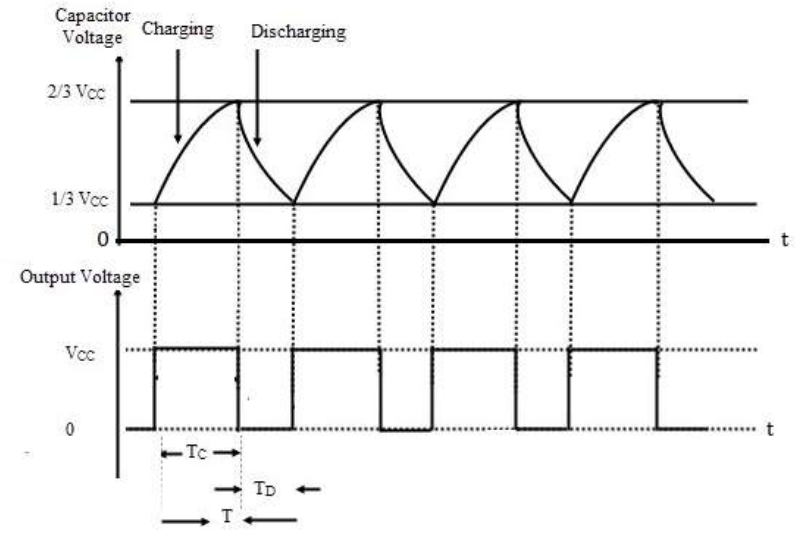
The above diagram represents IC 555 connected to R_A, R_B and C so as to form an astable multivibrator.

The internal resistance of IC 555 is generally 5kΩ, but in the above case it is 2R.

Since all the resistors have same value i.e. 2R the voltage drop across both the comparators would still be the same i.e. $1/3V_{CC}$ and $2/3V_{CC}$.

Hence, there would be no change in output waveform of the above given astable multvibrator irrespective of change in internal resistance.

The output waveform V_{OUT} and waveform across capacitor C is given as



Duty cycle of above circuit can be obtained as follows:

Duty cycle of astable multivibrator is given as follows

$$D\% = \frac{0.69(R_A+R_B)C}{0.69(R_A+2R_B)C} \times 100 \quad \text{....(1)}$$

Hence, $$D\% = \frac{(R_A+R_B)}{(R_A+2R_B)} \times 100$$

i) $R_A < R_B$

On substituting some random values for R_A and R_B such that $R_A < R_B$ in equation 1

For example a) let, R_A=2Ω, R_B=2.1Ω

$$\text{Then } D\% = \frac{(R_A+R_B)}{(R_A+2R_B)} \times 100 = \frac{(2+2.1)}{(2+2\times2.1)} \times 100 = 66.12\%$$

b) let, R_A=2Ω, R_B=1000Ω

$$\text{Then } D\% = \frac{(R_A+R_B)}{(R_A+2R_B)} \times 100 = \frac{(2+1000)}{(2+2\times1000)} \times 100 = 50.04\%$$

Hence value of D will lie between 50% and 66.66%.

ii) $R_A = R_B$

If value of R_A is equal to R_B, $$D\% = \frac{(R_B+R_B)}{(R_B+2R_B)} \times 100 = \frac{2}{3} \times 100 = 66.66\%$$

Hence when R_A=R_B duty cycle is 66%.

iii) $R_A > R_B$

On substituting some random values for R_A and R_B such that $R_B < R_A$ in equation 1

For example a) let, R_A=2.1Ω, R_B=2Ω

$$\text{Then D\%} = \frac{(R_A+R_B)}{(R_A+2R_B)} \times 100 = \frac{(2.1+2)}{(2.1+2\times2)} \times 100 = 67.21\%$$

b) let, R_A=1000Ω, R_B=2Ω

$$\text{Then D\%} = \frac{(R_A+R_B)}{(R_A+2R_B)} \times 100 = \frac{(1000+2)}{(1000+\ \times2)} \times 100 = 99.80\%$$

Hence value of D will lie between 66.66% and 100%.

Q.4.

a) Design a second order Butterworth high pass filter for cut-off frequency of 1 kHz and pass-band gain of A_F = 2. **(10)**

SOLUTION:

Data: f_o = 1kHz = 10^3 Hz

Pass-band gain A_F=2

Let us assume that R_2=R_3=R and C_2=C_3=C=0.01 µF

Step 1: Calculate value of R

$$R = \frac{1}{2\pi f_o C} = \frac{1}{2\times\pi\times10^3\times0.01\times10^{-6}}$$

R = 15.91 kΩ

Step 2: Calculate R_F and R_1

$$A_F = 1 + \frac{R_F}{R_1}$$

$$2 = 1 + \frac{R_F}{R_1}$$

$$\frac{R_F}{R_1} = 1$$

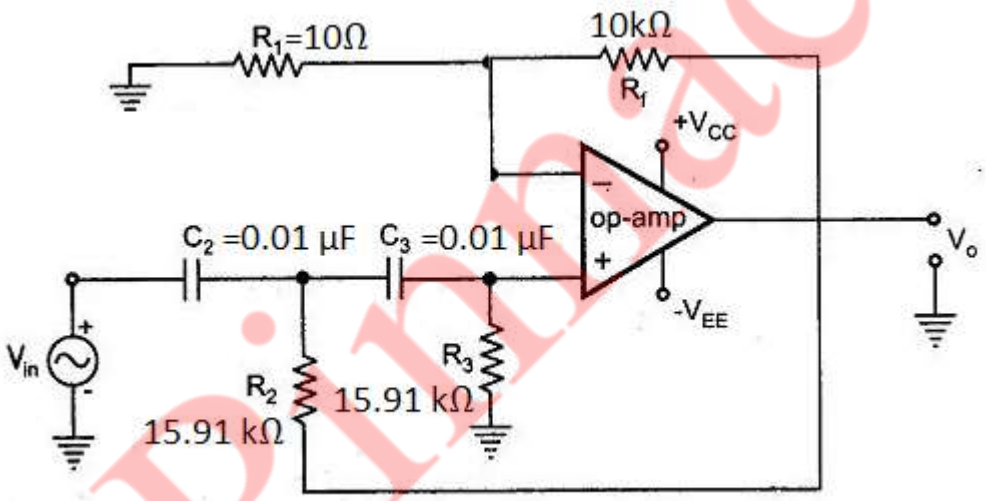
Let R_1=10kΩ

Hence R_F=10kΩ

Therefore, the components value are as follows

R_1=10kΩ, R_F=10kΩ
R_2=R_3=R=15.91 kΩ
C_2=C_3=C=0.01 µF

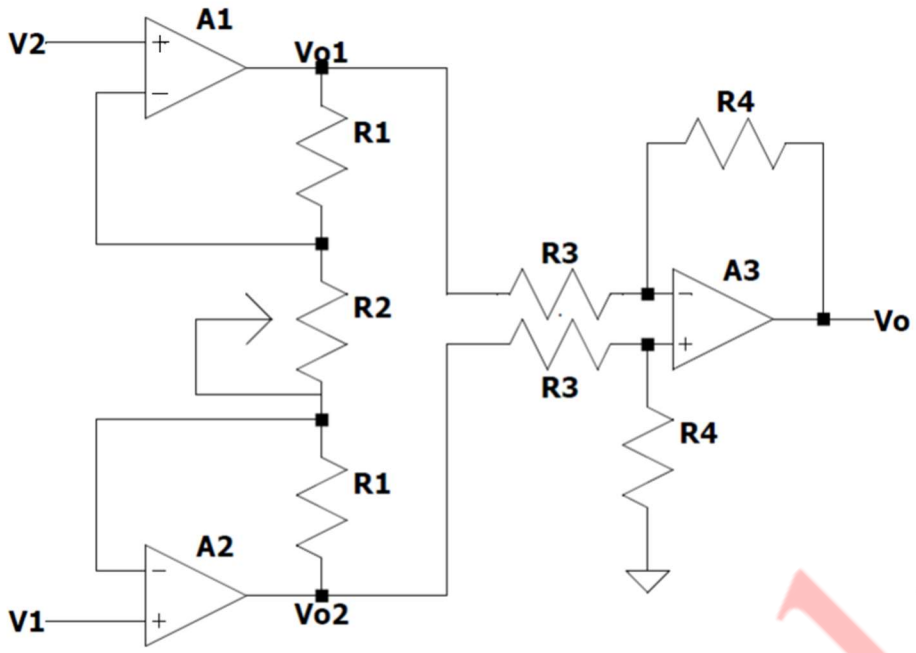
Step 3: Circuit diagram



b) With a neat circuit derive an expression for the output of an instrumentation amplifier. **(10)**

SOLUTION:

An instrumentation amplifier can be implemented using 3 op-amps as shown in the figure below.



Consider 3 op-amps A1, A2 and A3 where A1 and A2 act as non-inverting amplifier such that their inverting terminal (-) is connected to resistor R2 instead of ground.

The input impedance of all the op-amps (A1, A2 and A3) is assumed to be infinite, the currents flowing would be zero. Hence the current flowing through the

resistors R1, R2 and R3 is same i.e. 'I'.

Using the concept of virtual short we can obtain the voltages at nodes A and B as follows

$V_A = V_2$ and $V_B = V_1$

Hence the expression for current I is,

$$I = \frac{V_A - V_B}{R_2} = \frac{V_2 - V_1}{R_2}$$

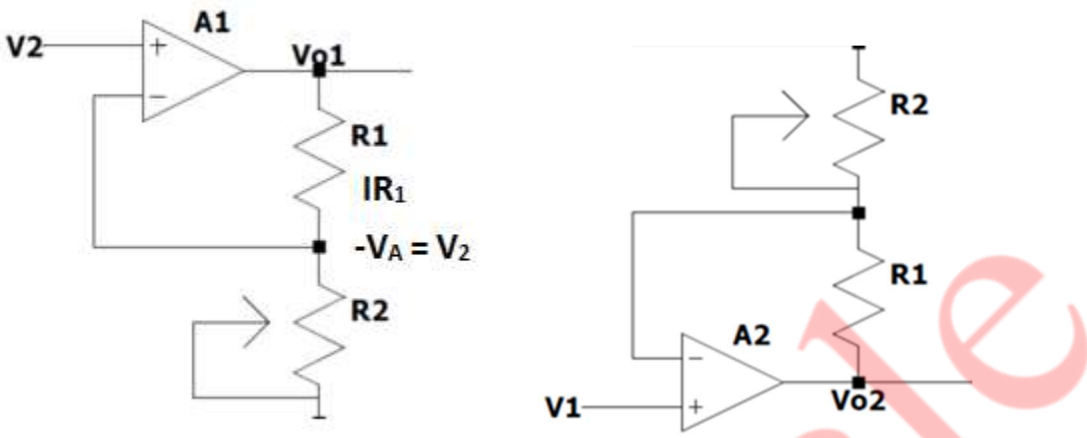
The output voltage of op-amp 2 (A2) is given by

$V_{o2} = V_A + IR_1 = V_2 + IR_1$

$$= V_2 + \left(\frac{V_2 - V_1}{R_2}\right)R_1$$

$$= \frac{V_2R_2 + V_2R_1 - V_1R_1}{R_2}$$

$$= \frac{(R_1 + R_2)V_2 - R_1V_1}{R_2}$$



The output voltage of OP-AMP1 is given by

$$V_{01} = V_B - IR_1$$

$$= V_1 - IR_1$$

$$= V_1 - \frac{V2 - V1}{R2} \times R_1$$

$$= \frac{V1R2 - V2R1 - V1R1}{R2}$$

$$= \frac{(R1 + R2)V1 - R1V2}{R2}$$

Hence the output of the first stage is given by

$$V_{02} - V_{01} = \frac{(R1 + R2)V2 - R1V1}{R2} - \frac{(R1 + R2)V1 - R1V2}{R2}$$

$$= \frac{(R1 + R2)(V2 - V1) + R1(V2 - V1)}{R2}$$

$$= \frac{(2R1 + R2)(V2 - V1)}{R1}$$

$$V_{02} - V_{01} = \left[1 + \frac{2R1}{R2}\right](V2 - V1)$$

Therefore, the gain of the first state is given by

$$A_{V1} = \frac{(V02 - V01)}{(V2 - V1)} = 1 + \frac{2R1}{R2}$$

The second stage is a difference amplifier with a gain of

$$A_{V2} = \frac{R4}{R3}$$

Therefore, the overall gain A_V of the three OP-AMP instrumentation amplifier is given by,

$$A_V = A_{V1} \times A_{V2}$$

$$\therefore \quad A_V = \left[1 + \frac{2R1}{R2}\right] \times \frac{R4}{R3}$$

Hence by using a variable resistor R_2 the overall gain can be easily and linearly varied.

The output voltage is then given by,

$$V_0 = A_V \times (V_1 - V_2)$$

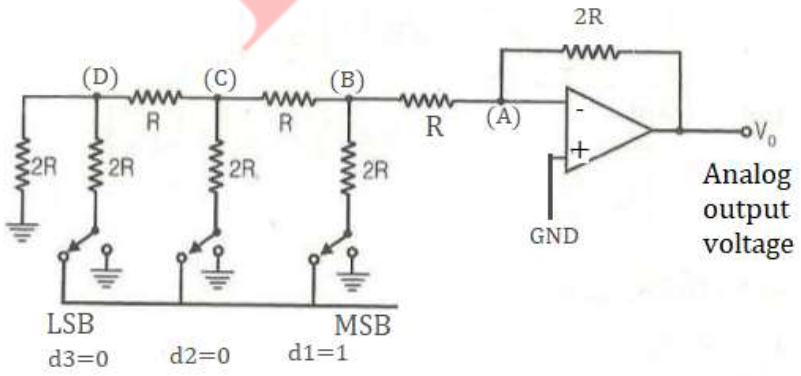
The triple OP-AMP instrumentation amplifier is available in IC form. For example, ICAD522 or INA 101. These devices will contain all the components except the variable resistance R_2 shown in the figure above.

Q.5.

a) With neat circuit explain R/2R ladder digital to analog converter. (10)

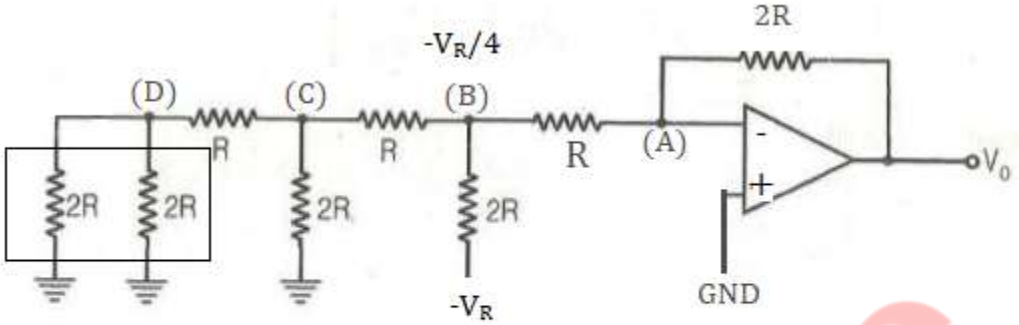
SOLUTION:

1. The circuit diagram for R-2R ladder DAC is as shown in figure below



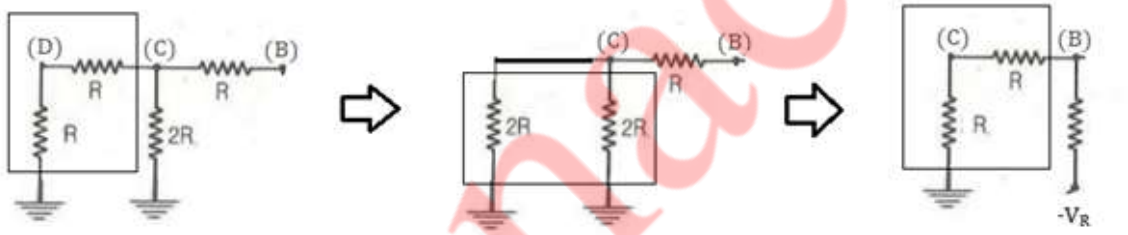
2. Unlike others wide range of resistors are not necessary to design a R-2R ladder DAC. Only two resistors R and 2R are needed hence the name.

3. This method is suitable for the realization of IC where the value of R can be anywhere between 2.5kΩ and 10kΩ but should not be less than 2.5kΩ.



Resistors in parallel
2R || 2R = R

FIG 1

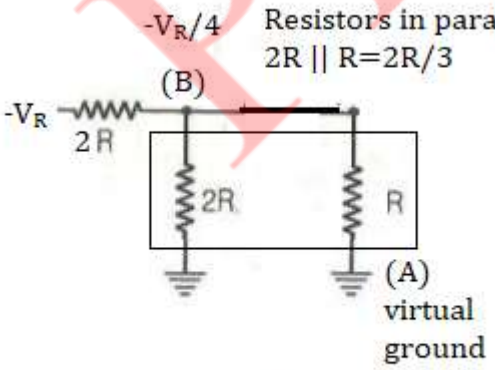


Resistors in series
R + R =2R

Resistor in parallel
2R || 2R = R

Resistors in series
R + R =2R

FIG 2



Resistors in parallel
2R || R=2R/3

FIG 3

Operation of R-2R ladder:

1. The number of digits per binary is assumed to be 3(i.e. n=3). The switch positions indicate that the binary word $d_1d_2d_3$=100.

2. The original circuit can now be simplified as shown in Fig.1 and Fig.2. Fig.1 gets further simplified into equivalent circuit as shown in fig.2.

3. The equivalent resistance to the left of node "B" in fig.1 is only 2R and node "A" is virtual ground potential.

4. The simplified final equivalent circuit is as shown in figure 3. In figure 3 as 2 resistors 2R and R are connected parallel to produce 2R/3.

5. Voltage at node "B" is given as

$$V_B=\frac{(\frac{2R}{3})}{2R+(\frac{2R}{3})}\times(-V_R)= -V_R/4$$

6. Hence the output voltage is given by

$$V_o=-\frac{R_f}{R_1}\times V_{in}=\frac{-2R}{R}\times\frac{-V_R}{4}=\frac{V_R}{2}=\frac{V_{FS}}{2}$$

Thus for binary input 100 the analog output produced is $V_R/2$.

7. Similarly analog output for other values of input digital value can be obtained.

d_1	d_2	d_3	Analog Output Voltage
0	0	0	0
0	0	1	$V_R/8$
0	1	0	$2V_R/8$
0	1	1	$3V_R/8$
1	0	0	$4V_R/8$
1	0	1	$5V_R/8$
1	1	0	$6V_R/8$
1	1	1	$7V_R/8$

Advantages of R-2R ladder DAC:

- Because we need resistors of only two values i.e. R and 2R, it os easier to build this circuit accurately.
- We can increase the number of input bits by just adding more

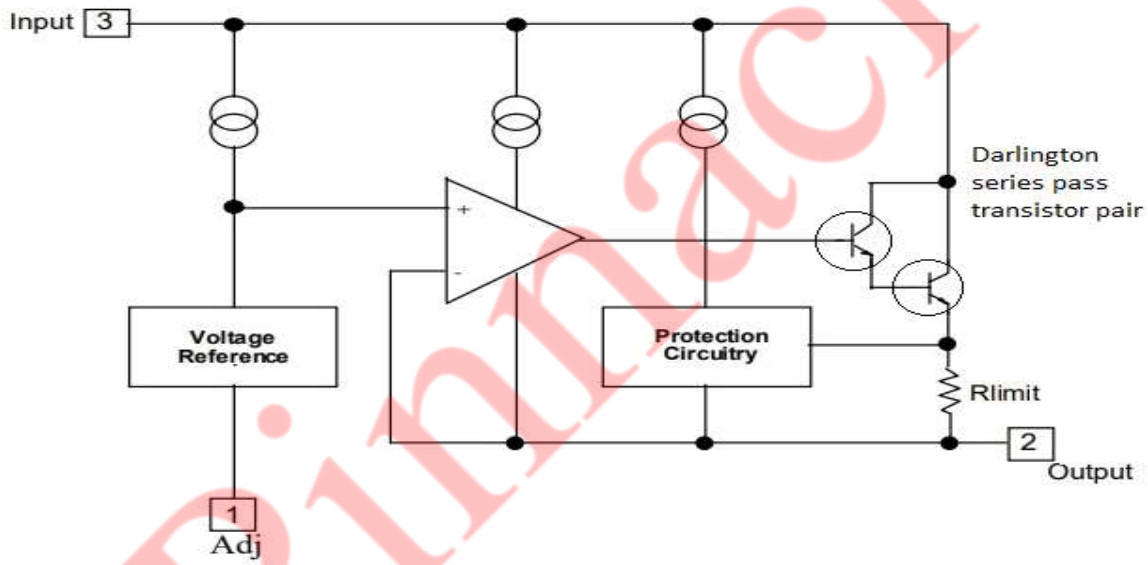
sections of same R/2R values.

- The equivalent resistance to the right of each labelled node (A,B,C,….) will be equal to 2R. Hence current flowing downwards, away from each node is equal to the current flowing towards right.
- Due to small resistance range required, the R-2R ladder can be fabricated monolithically, with a high accuracy and stability.

b) With the help of a functional block diagram explain the working of voltage regulator LM317 to give an output voltage variable from 6V to 12V to handle maximum load current of 500mA. (10)

SOLUTION:

1. Functional block diagram of positive adjustable voltage regulator LM 317 is as shown below



2. The functional block diagram above shows that LM 317 is a series regulator and a Darlington pair acts as a series pass element.

3. The output voltage is compared with the internally generated voltage reference to produce an error voltage which drives the Darlington transistor to regulate the output voltage.

4. R_{LIMIT} is an internal sensing resistance. The voltage across it is proportional to load current. This voltage is applied to the internal protection circuitry.

5. If the load current exceeds beyond its maximum value, the Darlington pair will be automatically turned off to protect the IC.

6. LM 317 is monolithic IC voltage regulator with an adjustable output voltage which can supply more than 1.5A current to the load. Its output voltage is adjustable over a range of 1.2V to 37V.

7. It employs the internal current limiting and thermal shutdown and safe area compensation.

Data: V_o = 6V to 12V

I_L(max) = 500mA

Let us assume maximum value of I_{ADJ} = 100µA and let R_1 = 240Ω.

1. Calculate minimum and maximum values of R_2

$$V_o = 1.25\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2$$

$$V_o = 1.25\left(1 + \frac{R_2}{240}\right) + 100 \times 10^{-6} \times R_2$$

For V_o = 6V i.e. minimum the corresponding value of R_2 will be R_{2min}

$$\therefore 6 = 1.25\left(1 + \frac{R_2}{240}\right) + 10^{-4} \times R_2$$

R_{2min} = 894.48 Ω

For V_o = 12V , value of R_{2max} will be

$$\therefore 12 = 1.25\left(1 + \frac{R_2}{240}\right) + 10^{-4} \times R_2$$

R_{2max} = 2025.24 Ω

Thus we want R_2 to vary from 894.48 Ω to 2025.24 Ω. Hence we choose R_2 to be a series combination of a fixed resistor of 680 Ω and a potentiometer of 1k Ω value.

2. To obtain 500mA, we should use TO-3 package with 20W power consumption rating.

3. Filter capacitors:

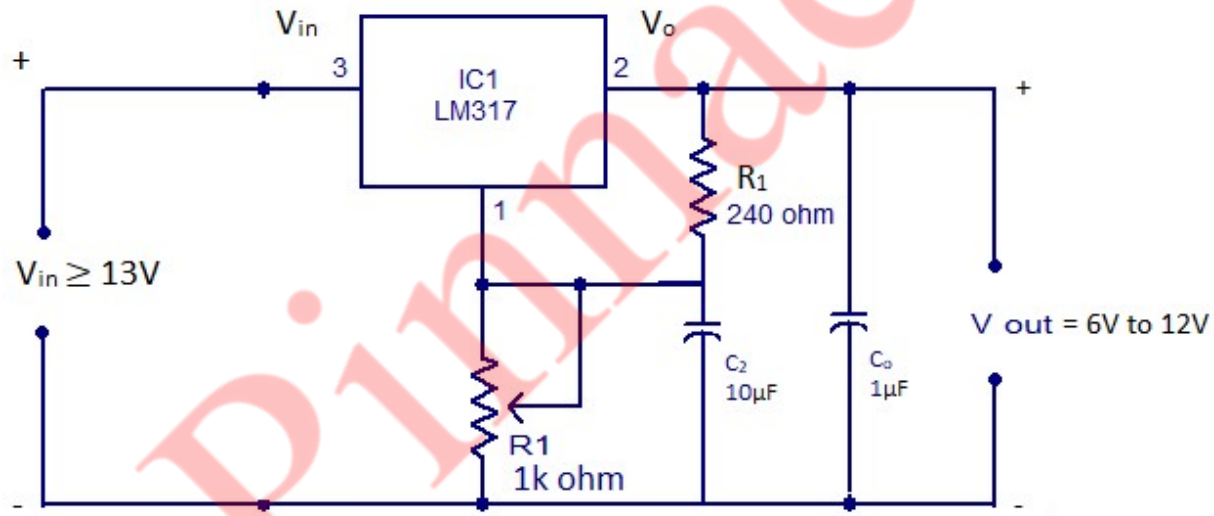
We assume that the regulator is close to the unregulated input supply. Hence the input capacitor C_i is not to be used. But for better ripple rejection use capacitor C_2 = 10µF between adjustment terminal and ground. The output capacitor C_o=1 µF is also being used.

4. Protective diodes:

As the output voltage is less than 25V and capacitors are smaller than 25µF, it is not necessary to use the protective diodes.

The minimum voltage drop across LM 317 is 3V. Hence the input voltage $V_{in} \geq 13V$.

Hence the complete designed Voltage regulator is as shown below:



Q.6. Short notes on: (Attempt any four)

a) Effect of swamping resistor. (05)

SOLUTION:

Swamping resistor are the resistors used to increase the input resistance of a differential amplifier connected in series to transistor and denoted by R_E'.

Effects of Swamping resistor are as follows:

1. The Q point gets shifted and needs to be readjusted.

2. The differential gain reduces substantially.

3. There is a considerable increase in the input resistance.

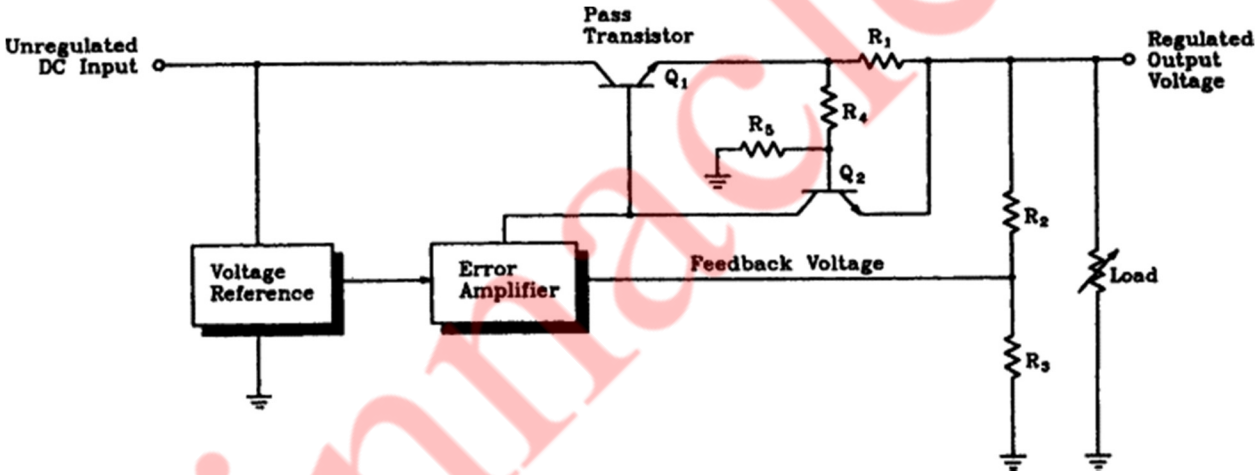
4. They minimize the effect of change in transistor parameters (e.g. h-parameters)

due to temperature, on the differential gain.

5. They also increase the linearity range of the differential amplifiers.

b) Current fold-back protection circuit in voltage regulator. (05)

SOLUTION:

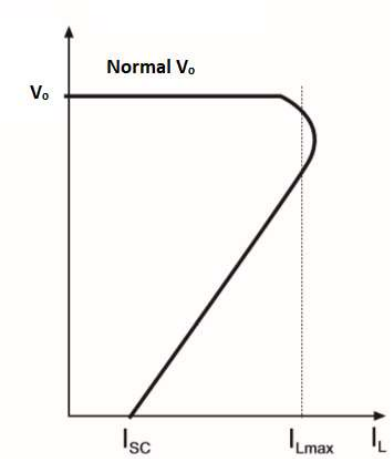


The circuit above shows a simplified circuit schematic of a discrete voltage regulator with foldback current limiting technique, which actually decreases the output current while operating in overload conditions.

The advantage of foldback current limiting is that it reduces the power dissipation taking place in the series pass transistor Q_1 under the short circuit condition as compared to power dissipation taking place in short circuit current protection.

As seen in the schematic above R_3 and R_4 are added to the short circuit protection.

Transfer characteristics of foldback current limiting circuit is as shown below



c) Voltage to current converter **(05)**

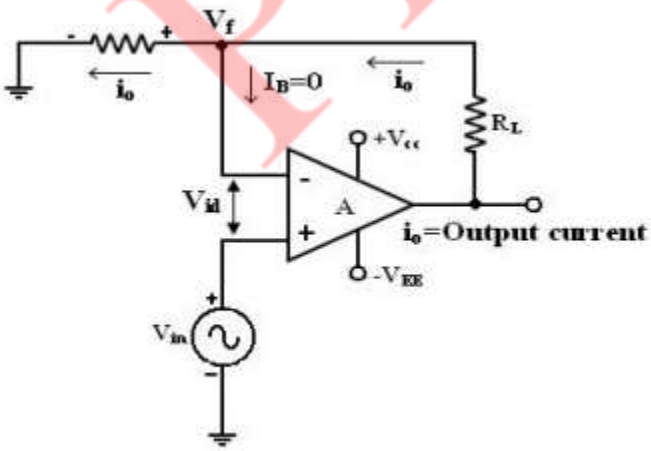
SOLUTION:

1. A voltage to current converter accepts the input in voltage form i.e. V_{in} and produces output in the form of current i.e. I_o. The output current is proportional to input voltage.

2. The voltage to current converter can be classified into two categories depending upon the position of the load.

- V to I converter with floating load.
- V to I converter with grounded load.

3. V to I converter with floating load:



Applying KVL to input loop $V_{in} = V_d + V_f$

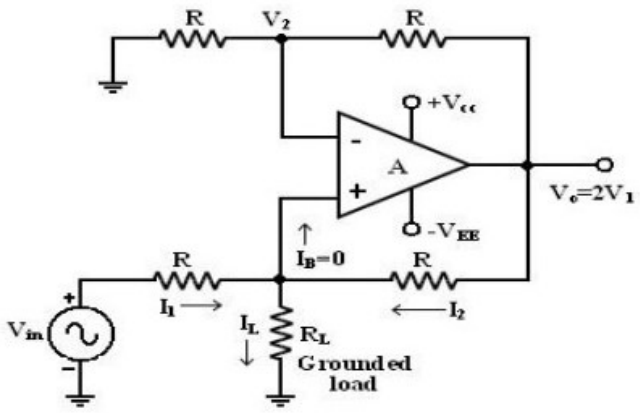
But since the open loop gain of op-amp is very large, $V_d=0$

Hence, $V_{in}=V_F$

But, $V_{in}=R_1 \times I_o$ …. (As $I_B \sim 0$)

Therefore, $I_o=\frac{V_{in}}{R_1}$

4. V to I converter with grounded load



Applying KCL at V_1 we get $I_L=I_1+I_2$

Where, $I_1=\frac{V_{in}-V_1}{R}$ and $I_2=\frac{V_o-V_1}{R}$

Putting this in above equation

$V_1 = \frac{V_{in}+V_o-I_L R}{2}$

$A_{VF}=2$ hence, $V_0=2V_{in}$

Therefore $I_L = \frac{V_{in}}{R}$

d) Peak detector circuit **(05)**

SOLUTION:

1. Peak detector is used to detect and hold the peak value of the input signal. Output of this circuit will follow the peak value of the input signal and store the maximum value infinitely.

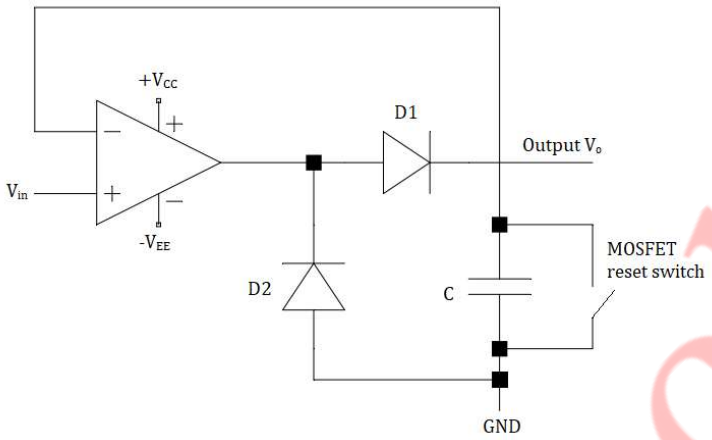
2. The two types of Peak detectors are as follows:

Positive peak detector

Negative peak detector

3. Positive peak detector:

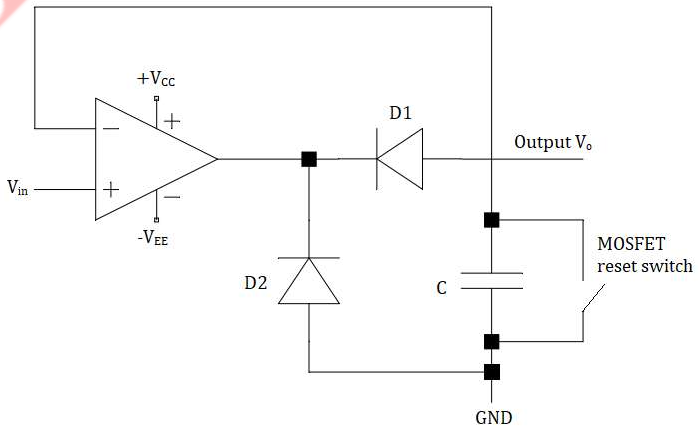
- Following circuit shows a positive peak detector using op-amp



- The op-amp is used as voltage follower. Hence the gain of the circuit is 1.
- The diode D_1 will be forward biased only in positive half cycle of the input, hence this circuit is sensitive only to positive input voltages.
- D_2 will not allow any negative voltage to go ahead. It will clamp negative output voltage to -0.7 volts (practical diode) or 0V (ideal diode).
- The diodes D1 and D2 are assumed to be ideal and the output voltage V_o is nothing but the output voltage across the capacitor i.e. $V_o=V_C$.
- This circuit can work in two modes: track mode and hold mde.

4. Negative peak detector:

- Following circuit shows a negative peak detector using op-amp

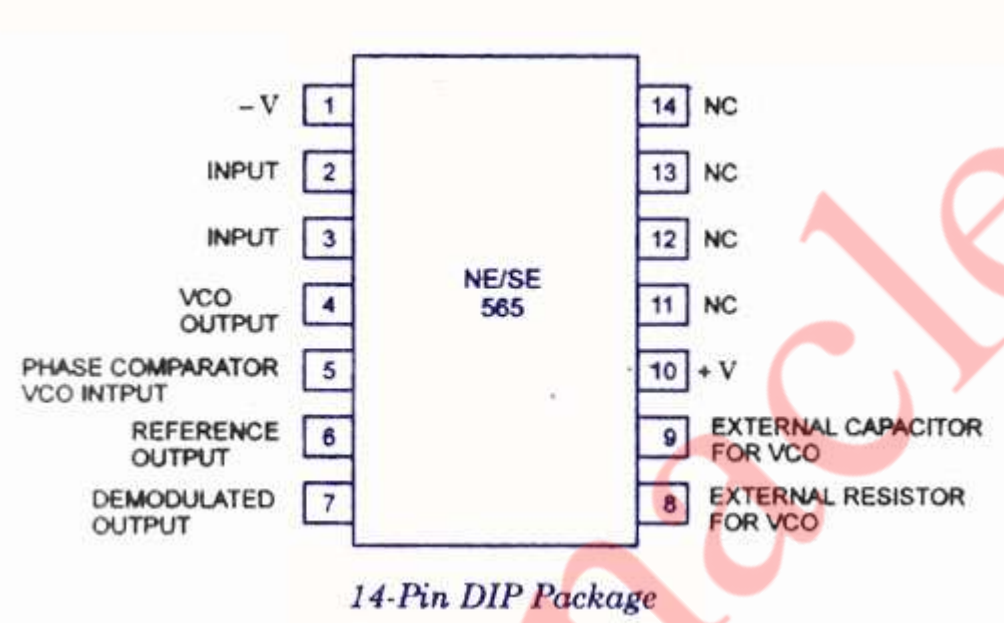


- By reversing the direction of the diodes the same circuit will operate as a negative peak voltage detector.

e) Working of PLL IC 565 **(05)**

SOLUTION:

1. PLL IC 565 is a 14 pin DIP and 10 pin metal can package. Pin configuration of 565 is as shown below



14-Pin DIP Package

2. Functional block diagram of IC 565 is as shown below

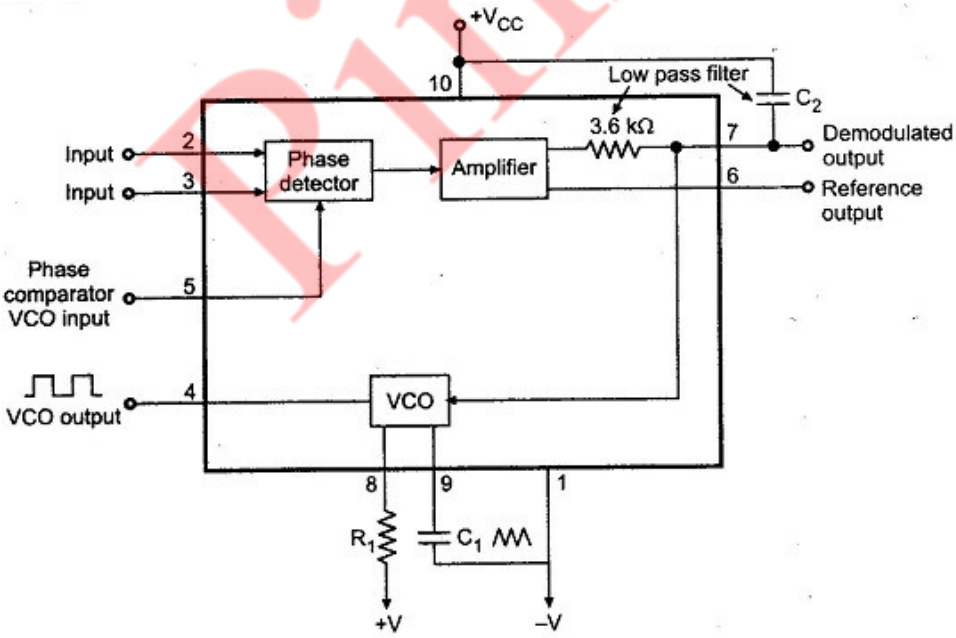


Fig. 2.125 Block diagram of IC 565 PLL

3. The free running frequency of VCO (i.e. when inputs 2 and 3 are grounded) is given by

$$f_o = \frac{0.3}{R_T C_T}\ Hz$$

Where R_T and C_T are externally connected components to pin 8 or pin 9 respectively as shown in functional block diagram.

This externally connected R_T can have a value between 2kΩ and 20kΩ whereas C_T can have any value.

4. To compare f_i and f_o pin 4 and pin 5 is connected externally.

5. The 3.6kΩ external resistor along with capacitor C connected between pin 7 and pin 10, such that value of this capacitor C should be sufficiently large to minimize variation in output at pin 7.

6. The 565 PLL is capable of locking to and tracking an input signal over ±60% bandwidth with respect to f_o (center frequency).

7. The lock range f_L of the PLL is given by

Lock range: $\Delta f_L = \pm \frac{8\, f_o}{V}\ Hz$

Where f_0= free running frequency of VCO in Hz

V=(+V) - (-V) volts.

8. The expression for the capture range is given by:

Capture range : $\Delta f_c = \pm \left(\frac{\Delta f_l}{(2\pi)(3.6)\times 10^3 \times C}\right)^{1/2}$

Where C is expressed in farads.